REMARKS

General

Reconsideration of the above-identified patent application in view of the amendments above and the remarks following is respectfully requested.

The abstract has been objected to as not being in the proper language and format. The abstract has now been amended to remove improper phrasing and includes less than 150 words.

A "Continuing Data" text, to be inserted on p. 1, line 1 of the specification is provided according to the Examiner's suggestion.

A corrected Figure 1 labeled "Replacement Sheets" is provided with this response.

Claims 41-82 are pending in the application. In the Office Action dated November 28, 2006, claims 53-64 were allowed, claims 42-52 and 67-78 were objected to and claims 41, 56 and 79-82 were rejected. Applicant gratefully acknowledges the allowance of claims 53-64 and the conditional allowance of claims 42-52 and 67-78. The Examiner's rejection is respectfully traversed.

The claims before the Examiner are directed toward data conversion methods and systems. The invention discloses in various embodiments a new data conversion method and architecture (apparatus) with applications in high-speed, high-resolution analog-to-digital conversion as well as in digital-to-analog conversion. The apparatus is termed "high-performance", wherein "performance" is clearly defined in the specification as relating to converter <u>resolution</u> (equivalent to dynamic range) and <u>speed</u> parameters (paragraphs 0015-0017 and 0045 of the published application). For example, paragraph 0045:

> The present invention discloses new data conversion architectures and methods, with applications to high-speed, high-resolution ADCs and DACs. In this description, "system", "apparatus" and "data conversion architecture" are used interchangeably. Also in the context of the present invention, the term "performance" represents the two basic data converter parameters: resolution and speed. *"High-performance" means high-resolution and high speed. "Low performance" means low-resolution or low-speed or both. Typical exemplary ranges for "high" and "low" are given below.*

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A main inventive feature of the apparatus and method relates to <u>digital frequency domain processing</u> as recited in paragraph 0018

> The architecture disclosed is essentially that of a wideband Nyquist converter (but can also be used for oversampling data converters). Advantageously, the method uses *frequency domain processing* (termed *"spectral"* processing herein) of an incoming signal. The architecture is general and can be applied to other than S/P arrangements, for example in the improvement of a DAC in FIG. 6 by using *frequency domain information* in an interleaving arrangement.

Another main inventive feature of the apparatus and method relates to the extraction and use of the frequency domain/ spectral information (for example for the frequency domain processing above, which is mainly digital), as recited in paragraph 0046:

> In contrast with time domain concepts that serve most prior art data converter architectures, the data conversion architectures and methods disclosed herein use frequency domain tools *to extract frequency domain information from the signal. This information is advantageously used in the processing of the signal, which is mainly digital.*

The frequency domain processing is described in detail, starting with FIG. 2.

§ 112 Rejections

Claims 79-82 were rejected under 35 U.S.C 112, second paragraph, as being indefinite for filing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The rejection is respectfuilly traversed. However, in order to expedite allowance, Applicant has amended the claim by removing the "whereby" clause

Claim 79 clearly now claims a method having two steps:

> *A method for implementing a high-performance data converter comprising the steps of:*
> *a. processing a time domain input signal into a frequency domain signal in a digital form using at least two data converters having each at least one lower performance parameter than the high-*

performance converter in order to obtain at least two processed signal; and

    b. recombining said at least two processed signals to obtain a final output signal from the high-performance converter.

The support for the frequency conversion recited in step (a) is found in the specification in paragraph [0082] :

> *"at the output (**FFTsum**) for combining several ADCs in parallel (to further increase sampling rate) by use of filter bank ADC methods". If only sampling speed increase is needed (like other Interleaving converters methods) then only the frequency domain processing can be used. It is known in the art that filter bank ADC methods require very high analog accuracies and stability (very small phase and gain errors). The frequency domain processing allows for high DR with relaxed analog accuracy requirements.*

Note that "filter bank" refers specifically to ADC (filter bank-ADC).

Applicant respectfully submits that the two steps clearly define an action of data conversion which in which an input signal is converted by the high-performance converter into an output signal. The conversion is performed coordinately by two converters each having lower-performance than the high-preformance converter. The processing is performed in the frequency domain. Applicant submits that obtaining conversion characterized by "high-performance" in the frequency domain through the use of two converters with lower performance capabilities is novel and inventive. Applicant thereby submits that claim 79 particularly points out and distinctly claims the subject matter which Applicant regards as the invention.

Applicant has amended claims 80 and 81 to remove unclear language referring to advantages and submits that these claims, which depend from amended claim 79, now similarly point out and distinctly claim the subject matter which Applicant regards as the invention. The same argument is applied to claim 82, which depends from claim 79.

§ 102(e) Rejections

Claims 41 and 66 were rejected under § 35 U.S.C. 102(e) as being anticipated by Killion et al (USPGPUB 2003/0091207), hereinafter "Killion".

Although not stated explicitly, claim 79 seems to have been rejected under § 35 U.S.C. 102(e) as being anticipated by Killion, since it appears under the 102(e) heading. The rejection is respectfully traversed. However, in order to more clearly distinguish the invention over the cited prior art, Applicant hereby amends claims 41 and 66 by adding "digital" to "frequency domain information". Support for the feature of the frequency domain information (and signals) being "digital" or "in digital form" is found throughout the specification, for example in paragraph 0050:

> *After digitization in ADC1, signal **330"** emerges as a converted first digitized output signal **332**, which is fed to spectral processor **306**. Advantageously, and in contrast with prior art conversion procedures, processor **306** performs at least one operation on digital signal **332** in the frequency domain and provides an analog "above-threshold" subtraction signal **334**, which is fed to subtractor **310**.*

and

> *ADC2 digitizes error signal **336** and outputs a second digital output signal **338**, which is also fed to spectral processor **306**. Advantageously and preferably, processor **306** processes signal **338** in the frequency domain and feeds the resulting frequency domain processed digital signals **340** (both "above-threshold" and "below-threshold" in FIG. 2) from both ADC1 and ADC2 to digital combining unit **314**. Unit **314** linearly recombines signals **340** to provide a final combined digital output **350**.*

In contrast, Killion discloses an analog-to-digital converter (ADC) suitable for hearing aid applications and which is used and useful for a single signal at the input, as explained below. Killion's invention is clearly targeted to hearing aids and the parameters relevant to such devices, chiefly among them the dynamic range. Killion states:

> *[0043] The quantization steps of the low-amplitude ADC are relatively small. The quantization steps are largest for the high-amplitude ADC. It can be argued that such large quantization steps are not detrimental to overall system performance since they are present only when signal amplitude is also large such that the overall signal-to- quantization noise ratio is favorable"*

Killion's two AD converters are distinguished by one being low amplitude and the other being high amplitude. The dynamic range of his hearing aid is clearly

restricted as understood from the following example: The maximum DR of a converter is the difference between the maximum, Full Scale (FS) signal and the Noise Floor (usually quantization noise and other distortions). A common way used in the art to demonstrate or measure the maximum (or "high") dynamic range (DR) of a data converter (ADC or DAC for example) is by use of multiple signals, for example two signals, one strong (near Full-Scale) and one weak (near the noise floor of the converter). In such a measurement, Killion's system will be dominated by the strong signal amplitude, with poor SNR (large ADC steps, see his FIG. 4 and the HIGH-AMPLITUDE ADC ONLY REGION 457). In other words, Killion cannot obtain a "high performance" signal as defined and claimed in the present invention even in his DR parameter.

Applicant submits that in order to get the maximum DR it is detrimental to have a maximum signal-to-quantization noise ratio when a large signal (near Full Scale) is present during measurment of maximum DR. In contrast, the present invention provides a very high DR (as demonstrated in FIGS.10(A-D) of the application).

In summary, Killion addresses a fundamentally different problem and discloses a converter that does not have and in fact is incapable of having a "high-performance" as defined in the present invention..

Specifically regarding the rejection of claims 41, 66 and 79: contrary to the Examiner's assertion, Killion does not disclose (with regard to claims 41, 66) a processing unit coupled to the conversion unit and operative to process digital frequency domain information extracted from said (time domain) signal and, based on said processed frequency domain information, operative to provide in combination with the conversion unit at least two processed signals; Killion does not disclose a recombining unit operative to combine said at least two processed signals into a single high-performance output signal. Similarly, with regard to claim 79, Killion does not disclose a method for implementing a high-performance data converter comprising the steps of processing a time domain input signal into a frequency domain signal in a digital form using at least two data converters having each at least one lower performance parameter than the high-performance converter in order to obtain at least two processed signals and recombining said at least two processed signals to obtain a final output signal from the high-

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performance converter;. <u>Killion's processing of signals is in the time domain</u>, using amplitude as a parameter. There are no digital frequency domain signals in Killion. In fact, there is no frequency domain processing of signals in Killion at all. Therefore, Killion does not anticipate any of claims 41, 66 and 79 because all three claims recite "digital frequency domain processing" as a key feature, and this key feature is simply missing in Killion. Moreover, Killion does not even render claims 41, 66 and 79 obvious, because he does not teach all of the claim limitations, and because, by processing his signals in the time domain he actually teaches away from the present invention.

§ 103(a) Rejections

Claims 80 and 81 were rejected under § 35 U.S.C. 103(a) as being unpatentable over Killion et al (USPGPUB 2003/0091207), in view of Pal (US 6,353,629). The rejection is respectfully traversed.
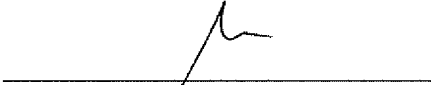
As indicated by Applicant above, Killion does not disclose the limitation of processing a time domain input signal into <u>a frequency domain signal</u> <u>in digital form</u> imposed on claim 79 and by dependency on claims 80,81. Killion does not teach the limitation of recombining the at least two (frequency domain) signals to obtain a final (frequency domain) output signal. Therefore, Killion does not teach or even suggest all of the claim limitations. Similarly, Pal does not teach frequency domain processing as defined and explained in detail in the present invention. Applicant submits that the Examiner mistakenly identifies a <u>time domain</u> equalizer (TEQ) realized as a tapped delay line via a Finite Impulse Response (FIR) filter (Pal, col. 6, lines 48-56) as a "filter bank ADC". Applicant submits that the TEQ has nothing to do with a filter bank ADC as defined in the present specification. Pal clearly indicates that his filter works in the time domain, not the frequency domain, and therefore clearly teaches away from the present invention. Therefore, Pal cannot and does not render claims 80 and 81 unpatentable. Since neither Killion nor Pal teach or suggest all of claims 80 and 81 limitations, and since both in fact teach away from the present invention by using <u>time domain processing</u>, the combination of Killion and Pal cannot render these claims unpatentable.

Objections

Claims 42-52 and 67-78 were objected to by the Examiner as being dependent upon a rejected base claim, but allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims. While gratefully acknowledging the conditional allowance of these claims, the objection is respectfully traversed, as Applicant argues that the respective base claims are allowable, and therefore these claims are allowable on their own

In view of the above amendments and remarks it is respectfully submitted that claims 41-82 are now in condition for allowance. Prompt notice of allowance is respectfully and earnestly solicited.

Respectfully submitted,

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